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High-Speed Board Design – A Fascinating Challenge for Hardware Designers

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Why is high-speed board designing on the rise?

Digitization being the need of the hour, every possible entity that can go digital has been digitized and this in turn has increased the amount of digital data to be processed, stored and transmitted.

- In past 5 years or so, the number of internet users have doubled with close to 50% of world population now having access to the world-wide web, which in turn demands an exponential increase in data rates, bandwidths and storage requirements.
- This rapid rise in digital data generation rate has paved way for revolutionary growth in data center technology oriented system designs.
- To meet this ever-increasing demand of higher data rates, high-speed connectivity interfaces are evolving day by day enhancing the data throughput.
    - PCIe Gen 4 supporting lane speeds up to 16 Gbps is out and PCIe Gen 5 boasting speeds up-to 32 Gbps is on the cards.
    - 24G SAS supporting speeds up to 24 Gbps per lane (proposed)
    - lane 100G interfaces supporting 25.78125 Gbps speed per lane
- Each of these evolving technology, in turn, triggers deployment of newer trends and techniques in board design making high-speed board design one of the hottest topics of hardware design cycle.
- The main challenge for hardware designers posed by this rapid increase in signal speeds is to deal with the design, especially PCB layout, in such a way that top notch signal integrity is ensured without skyrocketing the PCB fabrication cost

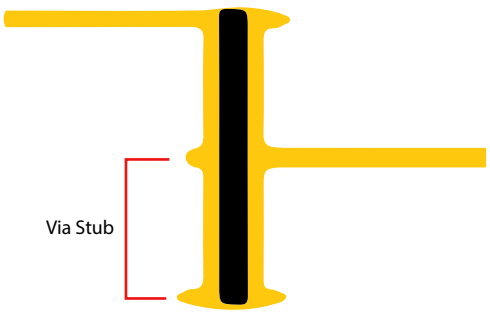
What should be kept in mind while starting the layout?

- The main point to be kept in mind is that the physical trace routed in the PCB is only half the path that high-speed current traverses. Equally important is the path that the return current flows in the signal's reference plane. The return path should be as continuous as possible. This also ensures that the current loop created by the signal is the smallest possible.
- Try to reduce impedance mismatches and stubs on the high-speed traces to the extent possible. Plan the layout such that high-speed signals have minimal layer transitions and proper terminations. Try to use high-speed SMD connectors or connectors with integrated impedance matching whenever possible.
- While placement, take care that the high-speed section is as far away from the noisy power supplies and switching elements as possible.
- Take utmost care while entering the constraints in schematics and layout. A clean and accurate constraint mapping ensures smoother routing and skew matching.
- Stick to guidelines and specification provided in the respective datasheets and design guides rather than applying thumb rules.

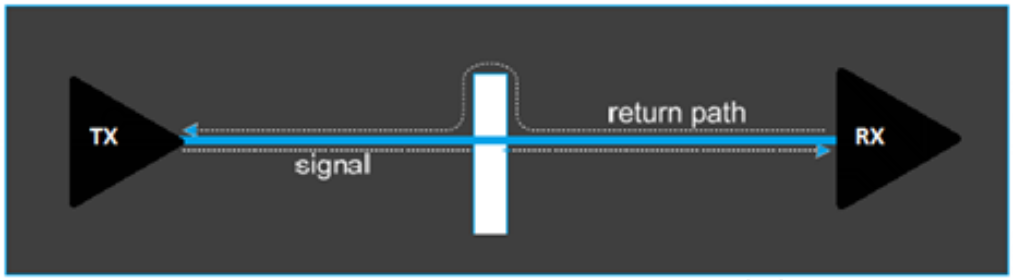
Why does high-speed PCB design pose a big challenge?

As propagation speed of a signal increases (rise time reduces), the distance across which the signal can be propagated over a medium without affecting the signal quality reduces (refer appendix for relation between propagation speed and dielectric). At high frequencies, the traces in PCB must be treated like a transmission line (refer appendix for an insight into transmission line concept). An ideal transmission line is impossible to realize and in practical scenario, impedance mismatches and related signal attenuation/distortions cannot be avoided. Some of the major reasons that lead to SI issues in a high-speed layout are but not limited to –

- Material dielectric and Trace length: The lower the dielectric, the lesser the attenuation. Dielectric material like Megtron and Rogers offer quite low dielectric values and are preferred for very high-speed boards where cost is of minimal concern. Also, having lower dielectric, in turn, allows greater trace lengths.
- Trace geometry, topology and pattern: Physical dimension of the trace such as width, length and height from reference plane have an impact on the overall trace impedance. Wider the trace and the closer it is to the reference plane, the lesser would be the inductance. However, this would increase the trace capacitance thereby affecting the drive strength required to propagate a signal.
  Trace impedance is also affected when it switches from one layer to the other. It would be nearly impossible to achieve the exact same impedance in all signal layers. So, for high-speed traces, it is always recommended to phase tune the traces in the same layer and as close as possible to the discontinuity. Bends and curves in traces are another source of impedance mismatch. The more the bends in a trace, the greater would be the discontinuities.
- Impedance mismatches introduced by through hole structures like vias, pins and ICT: Any through hole structure poses two threats to signal integrity – firstly, it obviously creates impedance mismatch due to its geometry and secondly, it introduces stub on the high-speed trace unless the signal is transitioning from top layer to bottom layer.



- SMD pads: Any component added to the trace will induce insertion loss. The impedance mismatch can be minimized by using components with smaller leads with widths comparable to trace width.
- Path of return current: Ideally, the return path should be a solid plane with no discontinuities so that the return current traverses the exact same path in the reference place as the trace carrying the signal. This would be the shortest possible loop. Any discontinuities in the reference plane like a split would force the signal to take an alternate path around the split, thereby increasing the loop length that can lead to EMI issues.



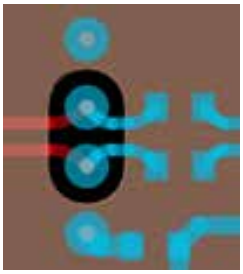
- Number of connectors: Board to board connectors are one of the major sources of signal distortion due to the impedance mismatch they introduce. The insertion loss and return loss induced are also considerable.
  High-speed connectors with embedded ground and impedance matching are recom mended for carrying high-speed currents.
- Stub length: These are quite dangerous and contribute much more to SI issues than other discontinuities. A considerably long unterminated signal stub can radiate energy like an antenna and contribute to signal distortion as well as EMI issues.

What are the popular trends and techniques used to overcome these challenges?

A few techniques that helps in mitigating some of the issues mentioned earlier follows.

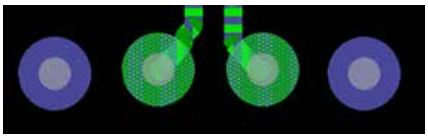
- Running phase tuning: High-speed differentials are phase tuned within the time-period (1/f) of the signal (Eg: around 600 mils for 10G signals in FR408) from the point of mismatch. This ensures proper common mode noise rejection.
- Reference plane voiding: Adjacent reference plane is voided under the component pads like AC coupling capacitors on the high-speed pairs. This compensates for the capacitance of pads and thereby reduces impedance mismatch.
- Component pad size: Packages with smaller lead lengths are preferred like DFN, QFN, LGA and similar. Coupling capacitors should be of 0402 or smaller dimension with 0201 preferred for frequencies above 5 GHz.

- Antipads for via and high-speed through hole pins: To reduce the mismatch induced by through hole structures, antipads are defined in all the layers for high-speed vias and through holes.



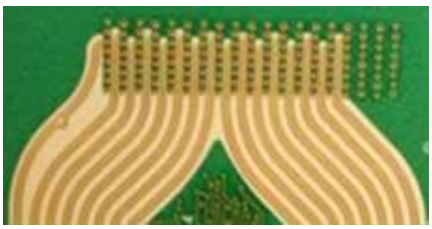
- Arc routing: In order to reduce mismatches due to angles and sharp bends in a trace, the traces are curved so that the trace width has minimum variation from the rest of the trace. Continuous reference plane: High-speed routes should have adjacent continuous reference planes without any split. If routing across split is unavoidable, stitching caps should be placed on either side of the pair to bypass the split.

- Ground Return Via: Whenever a high-speed signal switches layers and reference planes, adjacent ground stitching vias should be added in the vicinity of the differential vias in a symmetrical manner (refer following figure for recommended via placement). This ensures proper return path and reduces EMI emissions. An exceptional case is when the signal switches layers that share the same ground reference; Eg a switch from L1 to L3 with L2 being the reference plane for both L1 and L3. In this case, the return vias can be avoided.



- Unused pad suppression in inner layers: To reduce via/through hole impedance mismatch, unused pads are suppressed in all the internal layers. This also gives the advantage of increased real estate/clearance from via in internal layers.
- Reducing Via Stub: Buried and Blind vias or Back-drilling is used to avoid via stubs. If back drilling is not possible, signal routing should be planned to have minimum stub and 'U-turn vias' can be utilized to accomplish this as vias are considered a lesser evil than increased stub length.
- High-speed through hole connectors: Ensure that the ground pins sandwich the differential pairs while pinout is defined. High-speed press fit connectors usually have shorter lead length and are design so as to enable back-drilling of the through hole pads till point of contact.

- No Mask, No silk: Silk should not be placed over high-speed traces routed in outer layers to avoid slightest of mismatch. In certain boards used for test and measurement application, the high-speed traces are exposed (not covered by solder mask) so as to have minimum propagation delay.



Myths vs Reality

Differential pairs don't need ground reference: The ground plane is not just for maintaining the impedance of the differential pair. A differential pair can actually be considered as two different signals where in the current flow is equal and in opposing direction. For each of these signals, the return current would be flowing in the reference ground plane. Any split in the reference plane would force the return current to traverse through alternate path and will give rise to EMI issues. A lack of return vias whenever a high-speed differential pair switches layers will also lead to similar effect.

Ground vias/patch doesn't need clearance from the differential pair: The high-speed differential pairs need sufficient clearance from any copper structure including ground planes and vias. This is mainly due to the fact that any metallic structure closer to the differential pair can affect the overall impedance of differential pair.

Trace lengths and skews are limited to PCB: The trace length which is routed in the PCB is actually just the etch length and doesn't constitute the overall length traversed by the signal. The overall length includes the package lengths as well (length within the Chip package from the pins to the actual driver/receiver). So over all trace lengths of a signal includes the total etch length in PCB plus the package lengths of the transmitter and receiver ICs along with the package length of the connectors, if any. The skew matching of high-speed nets should also take into account the skews within the ICs and connectors as well.

Appendix

Propagation Speed: Electromagnetic waves propagate at speed of light in vacuum. This can be approximated to propagation speed of 11.8 in/nsec. For any other medium, the relative permittivity of the medium aka dielectric constant (Ɛr) of the medium comes into picture. The same holds true for the electrical signals propagating through a PCB trace.

Propagation Speed = 11.8/√Ɛr in/nsec; Ɛr = Ɛ/ Ɛ0

Where, Ɛ is the permittivity of the medium and Ɛ0 is the permittivity of free space or vacuum.
FR4, a commonly used PCB dielectric material, has an Ɛr of ~4.5 implying propagation speed in FR4 is approximately 5.6"/nsec (i.e. signal would take ~180 pico seconds to travel 1" in FR4)
For microstrip traces the dielectric constant is non-uniform as these have air on one side and dielectric of PCB material on the other. In this case the dielectric constant is generally approximated as

Ɛr' = 0.475Ɛr + 0.67; 2 < Ɛr < 6.

So, for FR4, Ɛr' = 2.57 implying faster propagation speed of ~7"/nsec (or propagation delay of ~140psec/in in FR4)

Lumped vs Distributed Systems:

For a lumped circuit element, like PCB trace, are physically small enough such that the voltage across and current flowing through every point of the element is uniform.
A distributed system is such that the voltage across the element is non-uniform and so current also varies along the conductor.
In terms of rise time (tr) and propagation delay (D), a circuit element is lumped if the effective length of rising edge,

$$l = tr/D < 6$$

i.e the system is lumped if the length is smaller than l/6. So, if a PCB trace is shorter than one sixth of the effective length of the rising edge, it can be treated as lumped.
For distributed systems, the transit time and phase changes of signals cannot be neglected and the element has to be impedance matched and terminated properly (has to be treated like a transmission line).

Transmission line concept:

An electrical transmission line can be defined as a pair of conductors designed to transmit alternating current and electromagnetic waves of Radio Frequency; currents with frequency high enough that their wave nature needs to be taken into account. Eg. Coaxial cable, twisted pair cable, microstrip and stripline traces geometries in PCB.

Electromagnetic waves with high frequency if transmitted over a normal conductor will attenuate as considerable amount of energy will be radiated off the conductor i.e. the conductor would behave like an RF antenna.

RF signals also tends to reflect from impedance discontinuities in the line such as connectors and joints and travel back down the line towards the source. This reflected wave hinders the transfer of the actual forward wave to the destination. The reflected wave can again get reflected back from the source as well and cause ringing and more signal distortions. This is one of the major source of radiated emission from an unterminated line.

Transmission lines, however, are designed using specialized construction such as precise conductor dimensions and spacing, and impedance matching so as to prevent the electromagnetic energy being radiated or reflected and minimize power loss. The most significant feature of a transmission line is that they have uniform cross sectional dimensions along their length, giving them a uniform impedance, the characteristic impedance Z0.

An ideal transmission line which is terminated by a purely resistive load with impedance equal to Z0 will transmit the signal without any loss from source to destination. Moreover, it will transmit the signal from one point to another in a fixed time irrespective of the rate at which the voltage changes.

$$Z0 = \sqrt{(L/C)}$$

Where,

Z0 is the characteristic impedance of the ideal transmission line,

L is the inductance per unit length of the ideal transmission line,

C is the capacitance per unit length of the ideal transmission line.

In practice, there will be losses in the transmission line due to the resistance of the conductor (R) and the conductance of the dielectric media between the conductors. So, practically,

$$Z0 = \sqrt{((R+j\omega L)/(G+j\omega C))}$$

Where,

Z0 is the characteristic impedance of the transmission line,

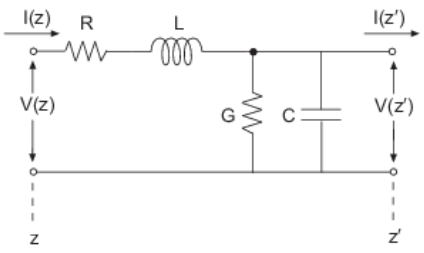
L is the inductance per unit length,

C is the capacitance per unit length,

R is the resistance per unit length,

G is the conductance of the dielectric per unit length,

$\omega=2\pi f$; The angular frequency.



Impedance of a microstrip:
Z0 =87/√(Ɛr+1.41)*ln(5.98H/(0.8W+T))

Impedance of a stripline:
Z0 =60/√Ɛr*ln (1.9H'/(0.8W+T))

Insertion loss: It is the loss of signal power in transmission line due to introduction of a device or component.

$$I\,R\,(dB) = 10\log_{10}\frac{P\,i}{P\,r}$$

Where,
IL is the insertion loss in dB,
PT is the power transmitted by the driver,
PR is the power received at the receiver after insertion loss.

Return loss: *It is the loss of signal power induced in the transmission line due to returned reflections from an impedance discontinuity like improper termination or addition of a component in the line.*

$$I\,L(dB) = 10\log_{10}\frac{PT}{PR}$$

Where,
IR is the return loss in dB,
Pi is the incident power,
Pr is the reflected power.

References:

1) *High Speed Digital Design: A Handbook of Black Magic by Howard Johnson and Martin Graham*
2) *https://en.wikipedia.org/*
3) *Right The First Time: A Practical Handbook On High-Speed PCB And System Design by Lee W. Ritchey*
4) *https://www.polarinstruments.com/*
5) *White paper on Signal Integrity by Technolution B.V.*

Author

Nithin Sathyan works with Happiest Minds Technologies as Technical Lead – Hardware. He has around 12 years of experience in high speed board design. He has hand on experience in dealing with high speed interfaces like 100G Ethernet, SAS-3 (12G), 10G Ethernet, PCIe Gen 3 and so on.

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