Case Study: Data acquisition FPGAs

Design of Data acquisition FPGAs supporting interfaces to ADC, DAC, discrete IOs, CAN, GPMC/PCIe/PC104

**BUSINESS REQUIREMENTS**
- Develop FPGAs supporting interfaces to ADC, DAC, discrete IOs, CAN
- Provide CPU interfacing over GPMC, PCIe or ISA in different variations of FPGA
- Simulation and on-board validation to be performed

**OUR SOLUTIONS**
- Verilog code for glue logic FPGAs to interface to CPU
- CAN controller IP from third party integrated
- Rigorous performance testing for all boundary conditions

**TOOLS/TECHNOLOGIES**
- Xilinx ISE/Vivado, Xilinx ISIM/Vivado simulator
- Verilog
- PCIe core, CAN controller IP core

**BUSINESS IMPACT**
- Strong protocol knowledge in PCIe/PCI/ISA/CAN and GPMC interfaces resulted in short design cycle
- Rigorous performance testing avoided field bugs
- Modular approach for internal registers and glue logic enabled code reusability with different interfaces

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About Happiest Minds Technologies

Happiest Minds, the Mindful IT Company, applies agile methodologies to enable digital transformation for enterprises and technology providers by delivering seamless customer experience, business efficiency and actionable insights. We leverage a spectrum of disruptive technologies such as: Big Data Analytics, AI & Cognitive Computing, Internet of Things, Cloud, Security, SDN-NFV, RPA, Blockchain, etc. Positioned as “Born Digital. Born Agile”, our capabilities spans across product engineering, digital business solutions, infrastructure management and security services. We deliver these services across industry sectors such as retail, consumer packaged goods, edutech, e-commerce, banking, insurance, Hi-tech, engineering R&D, manufacturing, automotive and travel/transportation/hospitality.

Headquartered in Bangalore, India, Happiest Minds has operations in the U.S., UK, The Netherlands, Australia and Middle East.

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