Case Study: NVMe 1.3 host bridge Verification using third party VIP

Functional Verification of an NVMe 1.3 Bridge FPGA code

**BUSINESS REQUIREMENTS**

- Develop a verification plan for functional verification of an NVMe 1.3 bridge FPGA
- Develop a testbench in UVM, integrate third party VIP, scripts and test cases for verification
- Execution and maintenance of test cases, help design team to debug RTL issues

**OUR SOLUTIONS**

- System Verilog and UVM based test bench, test cases with auto verification of 90% of the test cases
- Shell scripting for independent test case simulation and regression
- Parameterized execution for scalability and reusability

**TOOLS / TECHNOLOGIES**

- Mentor Questasim, Intel Arria 10, Linux, git, Shell script
- System Verilog, UVM, Verilog and VIP integration
- PCIe, NVMe 1.3 and AXI4 protocols, DDR4 memory models, NIOS II soft processor IP

**BUSINESS IMPACT**

- Full RAID group simulation reduced system level issues
- Proactive debugging realized faster time to market
- Improved functional coverage minimized field issues

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**Host Environment**

- PCIe Agent (0..1)

**Controller FPGA**

- Data & Management Interface

**DUT Environment (0..n)**

- NVMe bridge FPGA
- DDR4 Model
- NVMe + PCIe VIP

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Happiest Minds, the Mindful IT Company, applies agile methodologies to enable digital transformation for enterprises and technology providers by delivering seamless customer experience, business efficiency and actionable insights. We leverage a spectrum of disruptive technologies such as: Big Data Analytics, AI & Cognitive Computing, Internet of Things, Cloud, Security, SDN-NFV, RPA, Blockchain, etc. Positioned as ‘Born Digital . Born Agile’, our capabilities spans across product engineering, digital business solutions, infrastructure management and security services. We deliver these services across industry sectors such as retail, consumer packaged goods, edutech, e-commerce, banking, insurance, Hi-tech, engineering R&D, manufacturing, automotive and travel/transportation/hospitality.

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