

Functional Verification of PCIe Gen 5 IP using third party VIP as Root Complex and End Point

BUSINESS REQUIREMENTS



Develop a verification plan for functional verification of PCIe Gen 5 IP code targeting FPGA



Develop a testbench, integrate third party VIP, scripts and test cases for verification



Execution and maintenance of test cases, help design team to debug RTL issues

OUR SOLUTIONS



System Verilog based test bench, test cases with auto verification of 90% of the test cases



Perl and shell scripting for independent test case simulation and regression



Parameterized execution for scalability and reusability

TOOLS / TECHNOLOGIES



Mentor Questasim, Xilinx Vivado, Linux, Perforce, Shell and Perl script



System Verilog, Verilog and VIP integration



PCIe Gen 5 and AXI4 protocols, DDR4 memory models

BUSINESS IMPACT



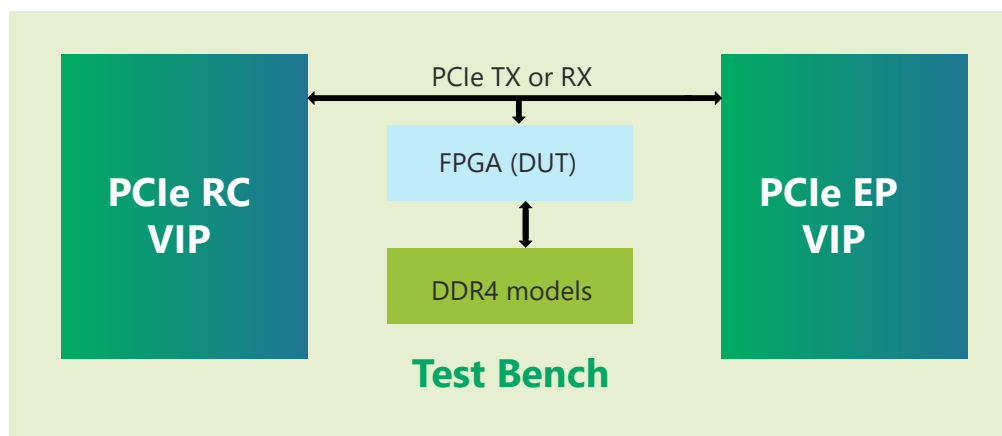
Strong domain knowledge and parameterized code development approach enabled the delivery of a future proof verification environment



Close co-ordination with design team helped to resolve issues promptly



Better functional coverage minimized number of bugs in the field



About Happiest Minds Technologies

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