Protocol/IP Validation **on FPGA Platform for a RISCV SoC**

01 BUSINESS REQUIREMENT:

- Prototype USB3.0, USB OTG and HEVC video codec IPs along with SoC RTL in multi-FPGA platform
- Simulate the modified RTL for functionality
- Validation of IPs on FPGA prototype hardware with bare-metal code
- Porting, integration and testing of USB3.0, USB2.0 OTG subsystem drivers in Uboot and Linux

02 OUR SOLUTION:

- Verilog code porting for interface/ IP bring-up and performance testing
- Redefined Clock Network for compatibility with Xilinx Ultrascale
- Achieved timing closure despite high resource utilization within FPGA
- Ported and customized USB 2.0 and USB 3.0 drivers from mainline kernel to board BSP

TOOLS /TECHNOLOGIES:

- proFPGA quad VUS prototyping platform, Xilinx Vivado, Cadence Xcelium simulator, Synopsys VCS simulator
- Verilog, System Verilog, UVM
- USB 3.0 multi host IP, USB OTG IP, HEVC video codec IP, AXI chip2chip over Aurora
- U-Boot 2020.07, Linux v5.5.0, Yocto Linux warrior

04 BUSINESS IMPACT

Expertise in pre-silicon validation aided in identifying and fixing of RTL bugs before SoC chip tape out

Timing closure expertise on highly dense FPGAs ensured complete SoC prototyping on given platform

Expertise in USB Linux framework ensured successful demonstration of USB use cases on FPGA platform
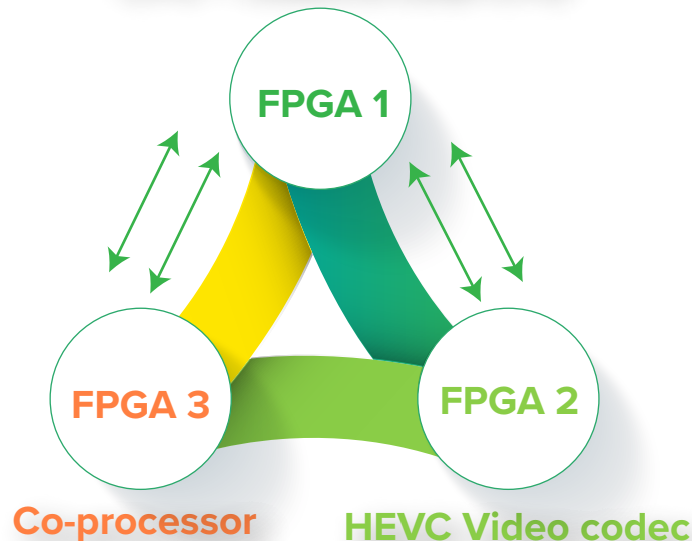
CPU + USB3.0/USB OTG

FPGA 1

FPGA 3

FPGA 2

Co-processor

HEVC Video codec

Figure 1: Multi FPGA platform

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